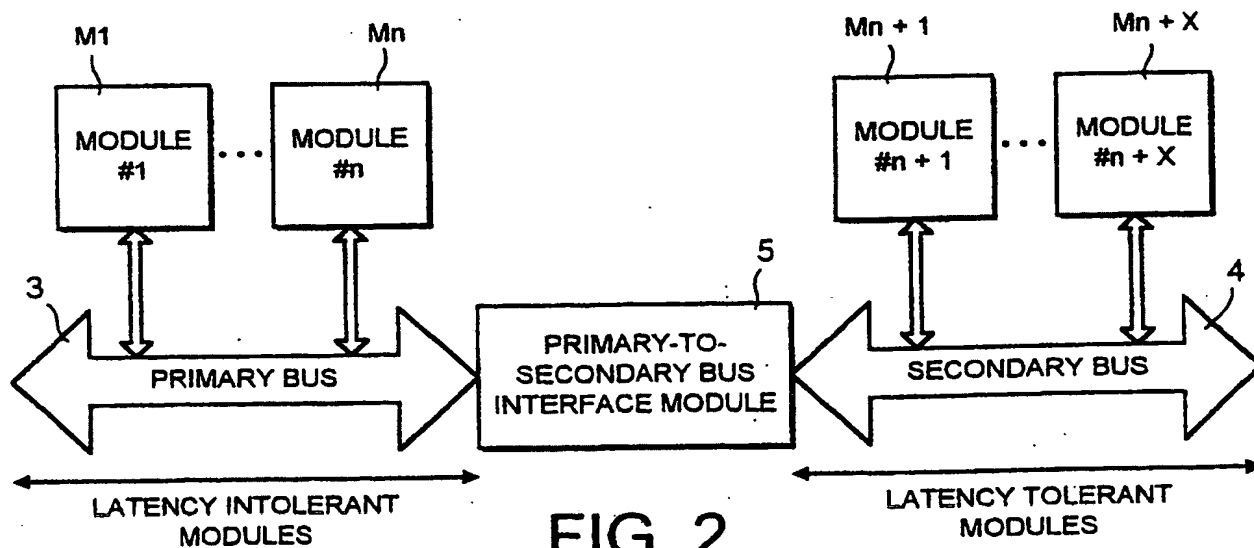


**FIG. 1**  
(PRIOR ART)



**FIG. 2**

7 / 16

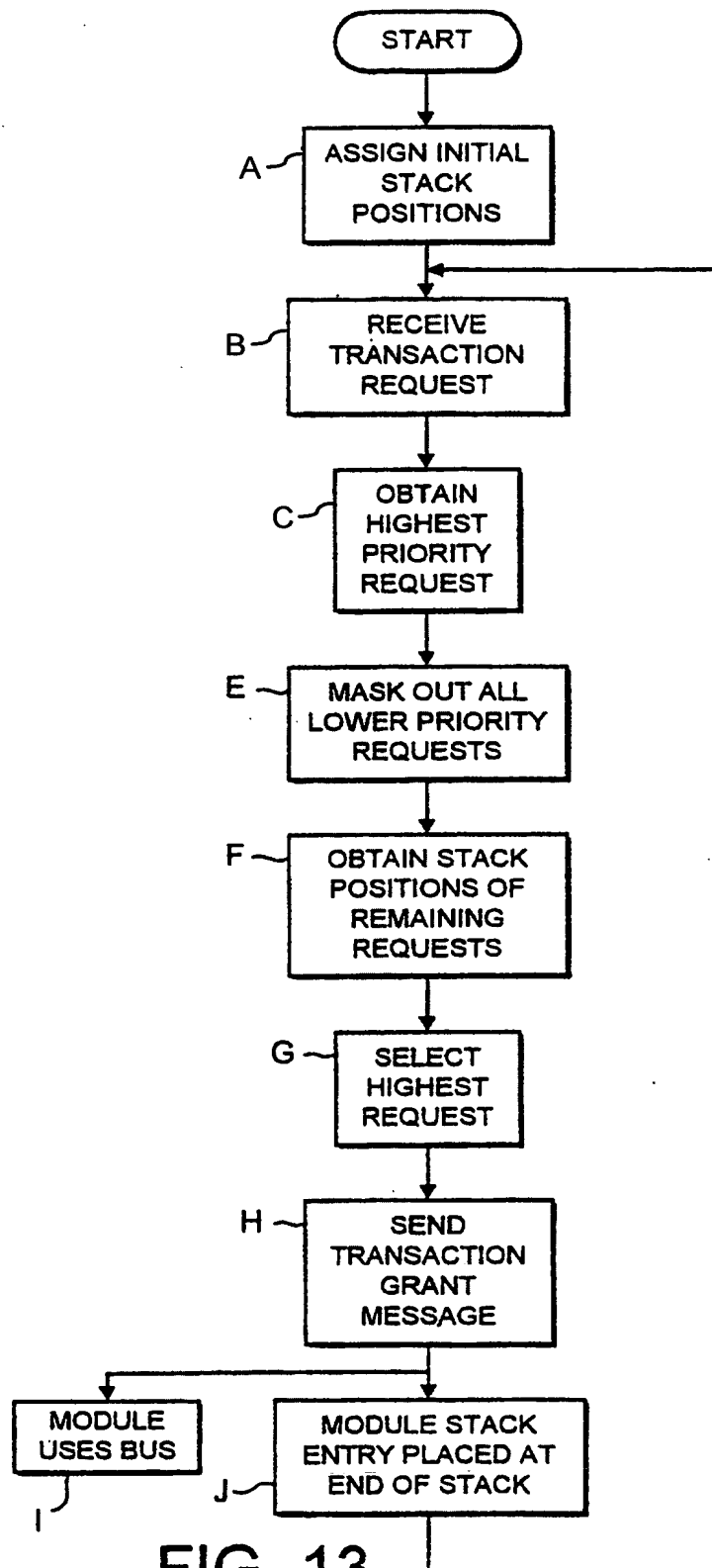
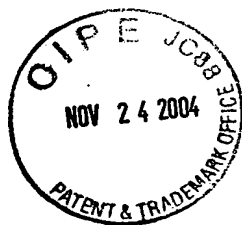


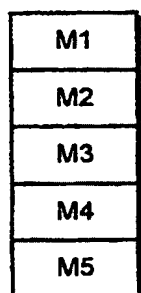
FIG. 13



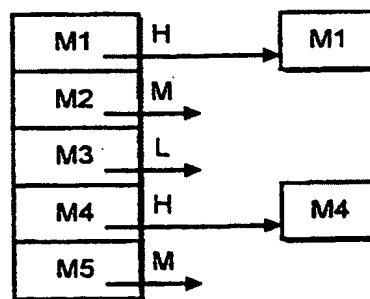
8 / 16

MODULE	PRIORITY
M1	H
M2	M
M3	L
M4	H
M5	M

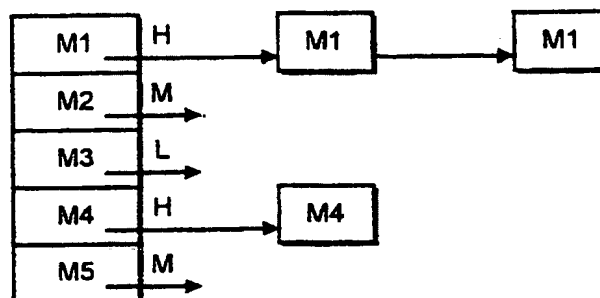
**FIG. 14**



**FIG. 15**



**FIG. 16**



**FIG. 17**

9 / 16

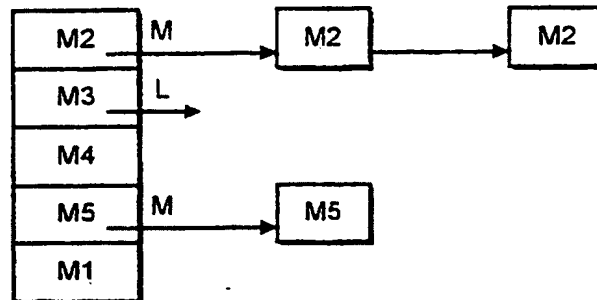
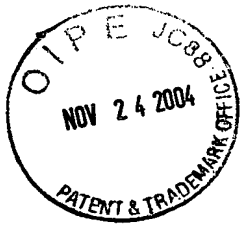


FIG. 18

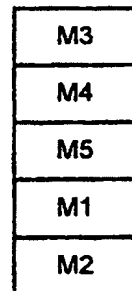


FIG. 19

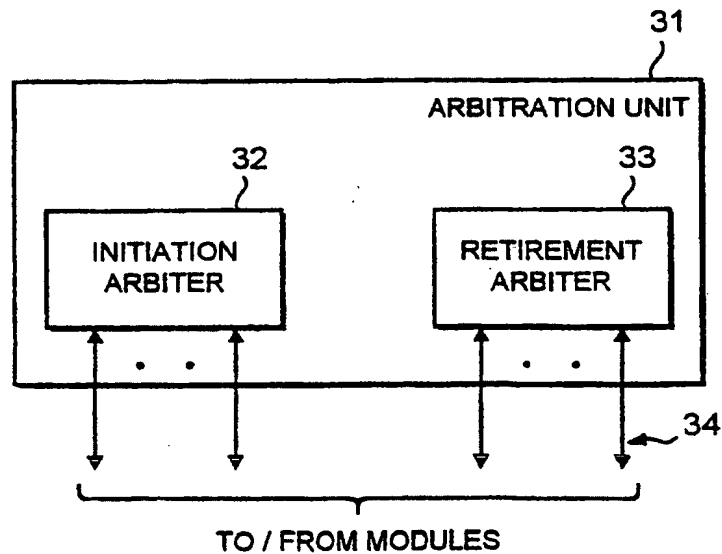


FIG. 20

10 / 16



T	R1	W1	R2	W2	R3	W3	....	
W		W1A	W1B	W2A	W2B	W3A	W3B	....
R				R1A	R1B			
TIME	t	t	t	t	t	t	t	

FIG. 21

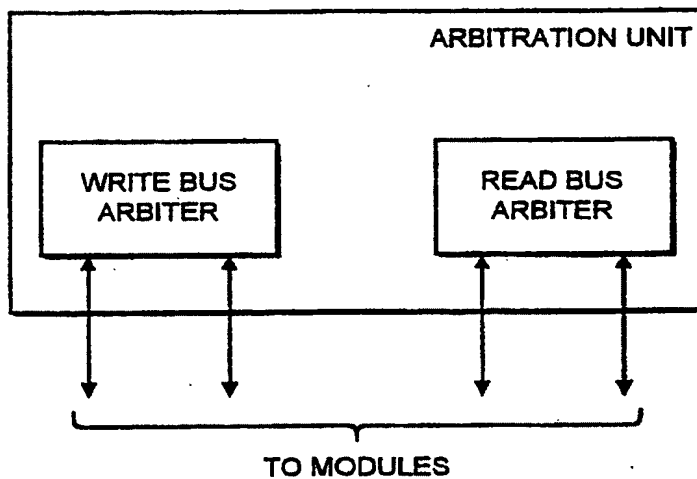


FIG. 22

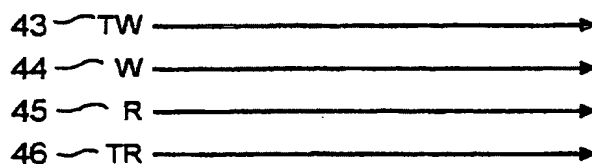


FIG. 23

12 / 16

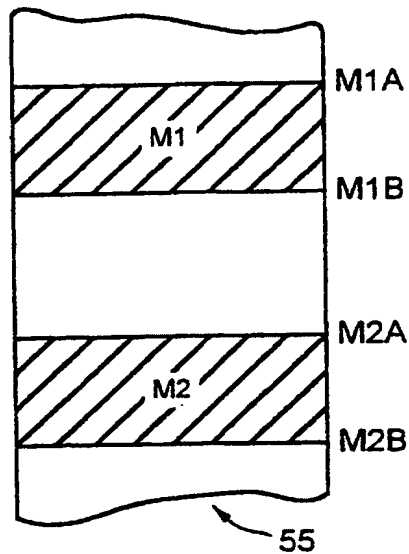


FIG. 26

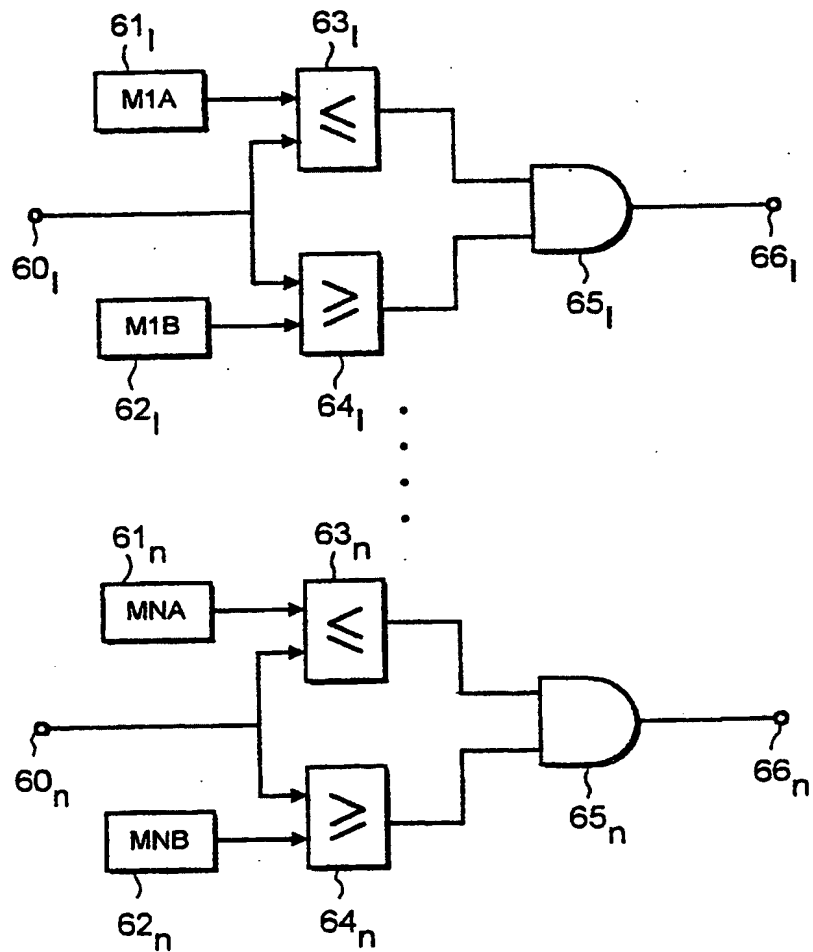


FIG. 27



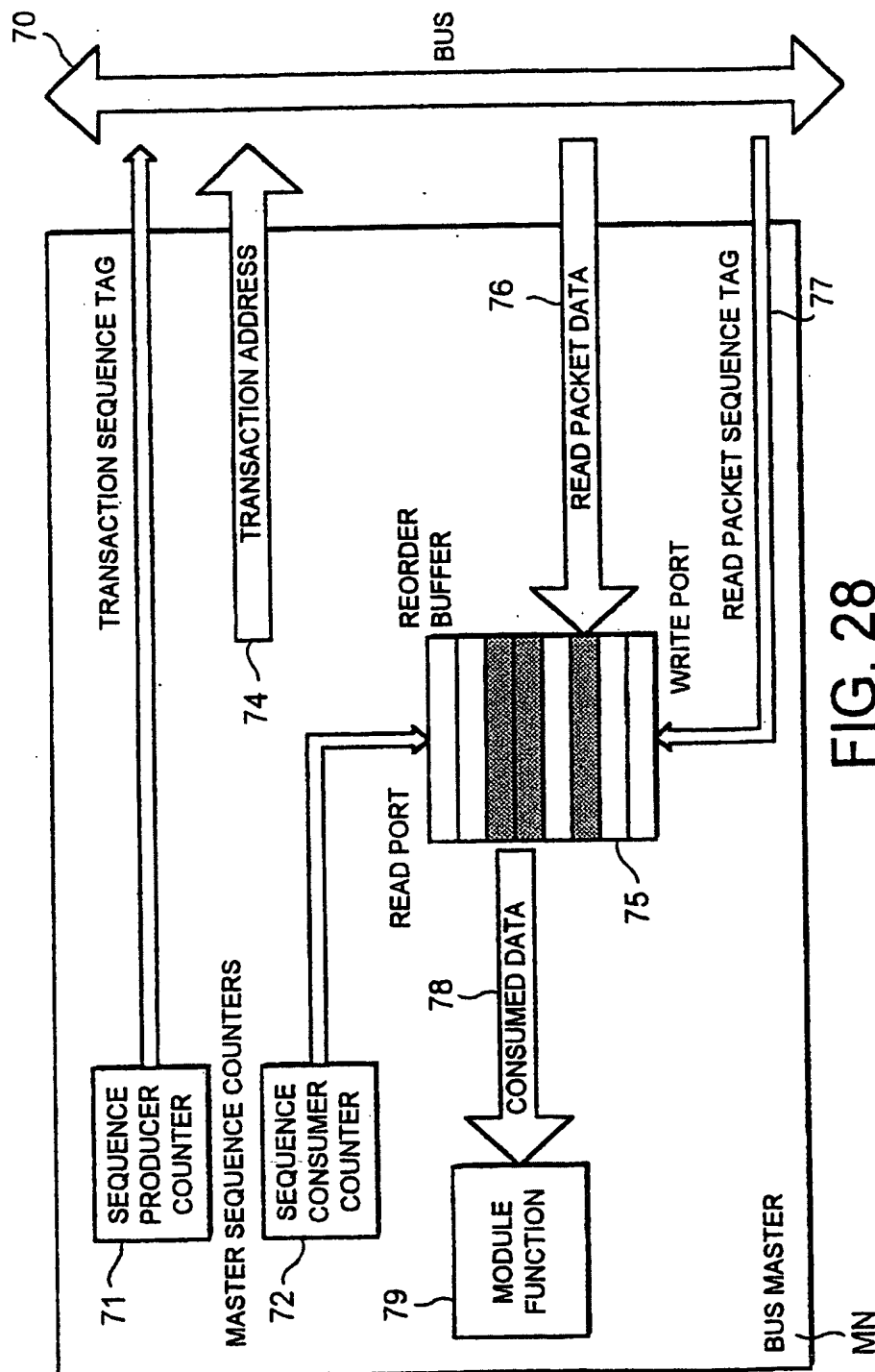
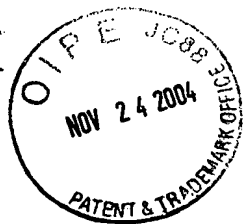


FIG. 28

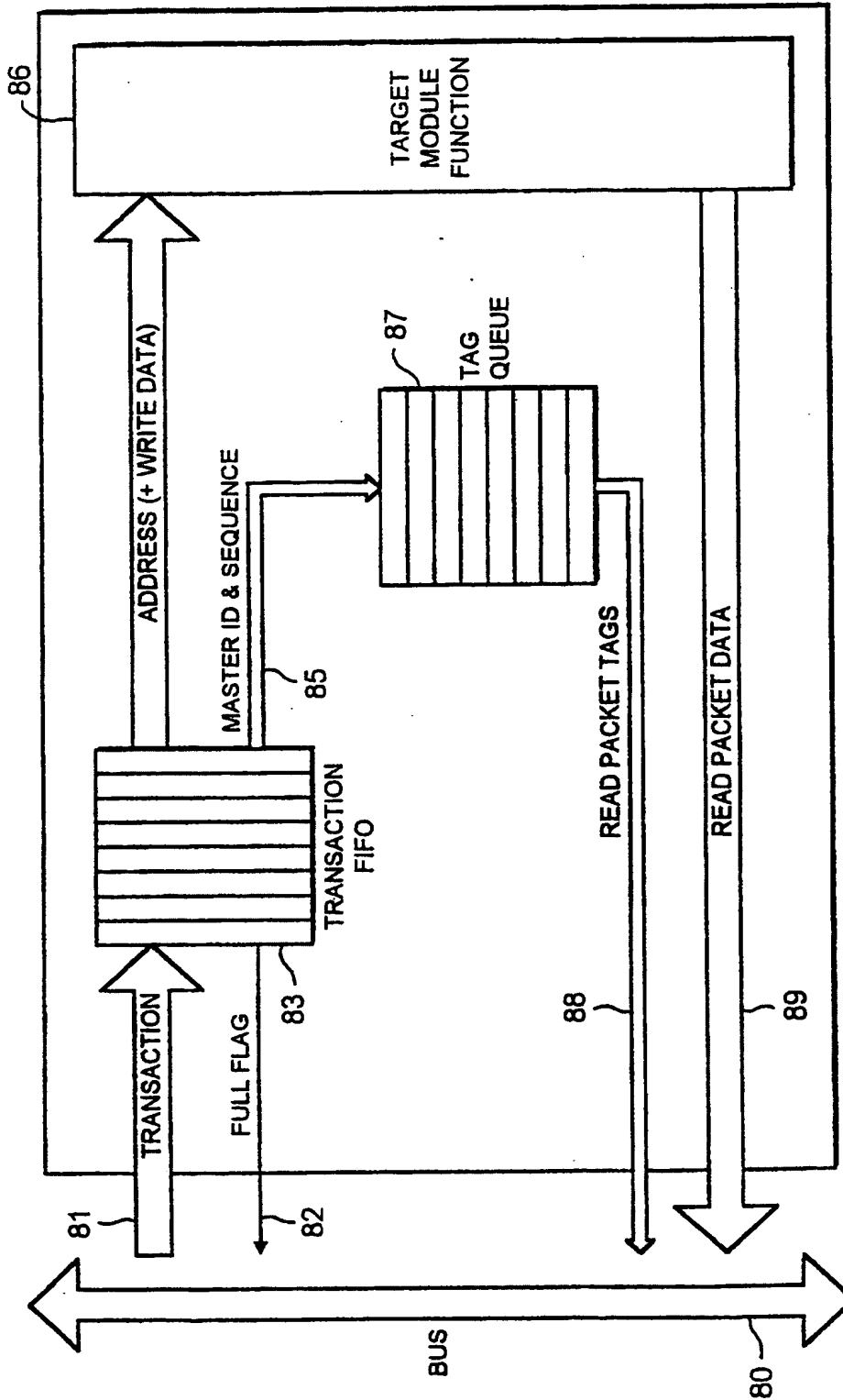
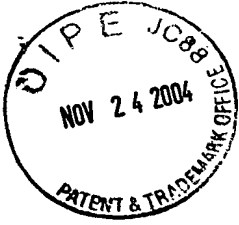


FIG. 29